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NOTIFICATION FOR FILING OPINION

Applicant: Kabushiki Kaisha Toshiba

Application No.: 10-2002-0008418

Title of Invention: Semiconductor Memory Device and Method of Manufacturing the Same

As the result of examination of the present application, the following reasons for rejection have been found and notified herein on the basis of the provision of Section 63 of the Patent Law. Any opinion about the rejection [Form 25-2 attached to the Regulations under the Patent Law], and/or any amendment [Form 5 attached to the Regulations under the Patent Law] must be filed by the above date. (The above date is extensible by one month for each request. No notification of allowance of extension of time will be issued.)

[Reason]

The invention described in claims 1 to 31 of the application is unpatentable under the provision of Section 29 (2) of the Patent Law, because it could be made before the filing of the present application, by any one who has ordinary knowledge in the art.

[Remarks]

1. Claims 1 to 26 describe a semiconductor memory device that has a main gate and an auxiliary gate. The memory device could be easily invented on the basis of cited invention 1 ("Analytical Surface Potential Expression for Double Gate SOI MOSFET," International Workshop on VLSI Process and Device Modeling, pp. 150-151 (May 14-15, 1999)), cited invention 2 ("Double Gate Poly Si TFT," Fourth Asian Symposium on Information Display, pp. 219-222 (Feb. 13-14, 1997)), cited invention 3 ("Double Gate SOI MOSFET,"